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Innovative Heterogeneous Design of Low Power Reconfigurable Router for Network on Chip (NOC)

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Abstract: *In this paper, objective is to first characterize the need of a heterogeneous reconfigurable router and show how an NoC built with reconfigurable routers allows the use of buffers with smaller depths. These in turn have a similar performance w.r.t. an NoC using a fixed size router, the latter showing a large buffer depth and incurring lower efficiency than the design presented here which can also lead to higher power consumption than the project design.*

Considering the NoC components, as crossbars, arbiters, buffers, and links, in the experiments realized by [4] the buffers were the largest leakage power consumers, dissipating approximately 64% of the whole power budget. In this way, the buffers can be considered as candidates for leakage power optimization by handling the buffers efficiently and effectively, since even at high loads, there can be 85% of idle buffers [4]. Regarding dynamic power, the buffers' consumption is also high, and it increases rapidly as the packet flow throughput increases [5].

Therefore, this paper particular goal is to provide an NoC router with a certain amount of heterogeneous reconfiguration logic, allowing changes in the amount of buffer utilization in each input channel, in conformity with the communication needs. The principle is that each input channel can lend/borrow buffer units to/from neighbouring channels in order to obtain a determined bandwidth. When a channel does not need its entire available buffer, it can lend buffer word slots to neighbouring channels. The inefficiency in the amount of buffers used within a homogeneous router, and the gains that can be achieved using the proposed strategy can be shown at further level. The focus is on providing a reconfigurable router that can be tested to optimize power and improve energy usage while sustaining high performance, even when the application changes the communication pattern.

Keywords: *Network on Chip (NoC); Heterogeneous Reconfigurable Router; First in First out (FIFO) Buffer; Crossbar Switch; Channel / Control Logic; Register Transfer Level (RTL) Design, Low Power, Low Area , Throughput ,Latency ,Critical time path.*

I. Introduction

Multiprocessor System-on-Chips (MPSoCs) are emerging as one of the technologies providing a way to support the growing design complexity of embedded systems, since they provide processor architectures adapted to selected problem classes, allied to programming flexibility.

To ensure flexibility and performance, future MPSoCs will combine several types of processor cores and data memory units of widely different sizes, leading to a very heterogeneous architecture.

The increasing interconnection complexity and the known scalability deficiency of buses require another model of interconnection. The communication among cores of an MPSoC having reusable and scalable interconnections is being provided by networks-on-chip (NoCs) [1]. NoCs have been proposed to integrate several Intellectual Property (IP) cores, providing high communication bandwidth and parallelism. Scalable bandwidth requirement can be satisfied by on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC) architecture. The basic idea came from traditional large-scale multi-processors and distributed computing networks.

The scalable and modular nature of NoCs and their support for efficient on-chip communication lead to NoC-based system implementations. Even though the current network technologies are well developed and their supporting features are excellent, their complicated configurations and implementation complexity make it hard to be adopted as an on-chip interconnection methodology.

Therefore, this project's particular goal is to provide an NoC router with a certain amount of reconfiguration logic, allowing changes in the amount of buffer utilization in each input channel, in conformity with the communication needs. The principle is that each input channel can lend/borrow buffer units to/from neighbouring channels in order to obtain a determined bandwidth. When a channel does not need its entire available buffer, it can lend buffer word slots to neighbouring channels. The inefficiency in the amount of buffers used within a homogeneous router, and the gains that can be achieved using the proposed strategy can

be shown at further level. The focus is on providing a reconfigurable router that can be tested to optimize power and improve energy usage while sustaining high performance, even when the application changes the communication pattern.

II. Literature Review

Network on Chip or Network on a Chip (NoC or NOC) is a communication subsystem on an integrated circuit (commonly called a "chip"), typically between Intellectual Property (IP) cores in a System on a Chip (SoC).

Nowadays System-On-Chips (SoCs) have evolved considerably in term of performances, reliability and integration capacity. The last advantage has induced the growth of the number of cores or Intellectual Properties (IPs) in a same chip. Unfortunately, this important number of IPs has caused a new issue which is the intra-communication between the elements of a same chip. To resolve this problem, a new paradigm was introduced i.e. Network-On-Chip (NoC). Since the introduction of the NoC paradigm in the last decade, new methodologies and approaches have been presented by research community and many of them have been adopted by industrials. The objective of the works done was to establish a reliable survey about available designs, simulation or implementation. An important amount of information was hence collected which characteristics NoCs dedicated architecture that will be presented throughout this literature survey. This survey is built around a respectable amount of references and it is hoped that it will help realise the model that is to be designed here.

A variety of interconnection schemes are currently in use, including crossbar, buses and NOCs. Of these, later two are dominant in research community. However buses suffers from poor scalability because as the number of processing elements increases, performance degrades dramatically. Hence they are not considered where processing elements are more. To overcome this limitation attention has shifted to packet-based on-chip communication networks, known as Network-On-Chip (NOC).

A typical NoC consists of computational **processing elements (PEs), network interfaces (NIs), and routers.** The latter two comprise the communication architecture. The NI is used to packetize data before using the router backbone to traverse the NoC. Each PE is attached to an NI which connects the PE to a local router. When a packet was sent from a source PE to a destination PE, the packet is forwarded hop by hop on the network via the decision made by each router. For each router, the packet is first received and stored at an input buffer. Then the control logics in the router are responsible to make routing decision and channel arbitration. Finally, the granted packet will traverse through a crossbar to the next router, and the process repeats until the packet arrives at its destination.

III. Differences Between Proposed And Original Reconfigurable Router :

1. In our reconfigurable router design, even if a channel is taking data from its neighbouring channel it will continue to take the packet input at its own channel. This is not so in the router designed in the reference paper where once a channel starts accepting packets from its neighbor (left or right) it will not take any packet input directly to that channel. So, it will support heterogeneous data.
2. Addition of two tag bits to the packets or flits(in wormhole switching) before storing them in the FIFO to indicate the channel to which this packet or flit was input.'00' for packets coming directly to the concerned channel,'01' for packets coming from the right neighbor and '10' for packets from the left neighbor.
3. Use of tag bits for indicating the direction of output from the crossbar.In an 8 bit packet ,the first two bits are used to indicate the address of the next router on the NOC.
4. We have implemented the control circuit by including features like acknowledge for writing ,acknowledge for reading, request and grant signals for writing in another channel's FIFO

IV. Proposed Work

In the proposed heterogeneous reconfigurable router, the major change in the architecture of router is channel architecture . The channel of the router is designed in such a way that it can store heterogeneous data in comparision of layered data in original router by adding tag bits. Here the NoC efficiency can be increased as a function of the possibility to reconfigure the buffer size according to the requirements of each channel of the router at run time, without the need to oversize buffers to guarantee performance.

In this work, designing the block diagram as shown in Fig. 1. is the first step taken. Designing the block took ideology from the previous versions of homogeneous routers that had all the resources allocated at static time and those couldn't be altered at the design run time which posed problem of longer bit data rejection when used at different communication channels and hence was ineffective in handling different versions of flowing data. Then second step was using a Hardware Description Language (verilog in this project) to help realise the project to be environment ready that is to conceptualise the ideology so that it can be fulfilling for

further steps. Thirdly, to be ready for real time industrial environment the HDL file was then made to simulate to obtain the optimum result.

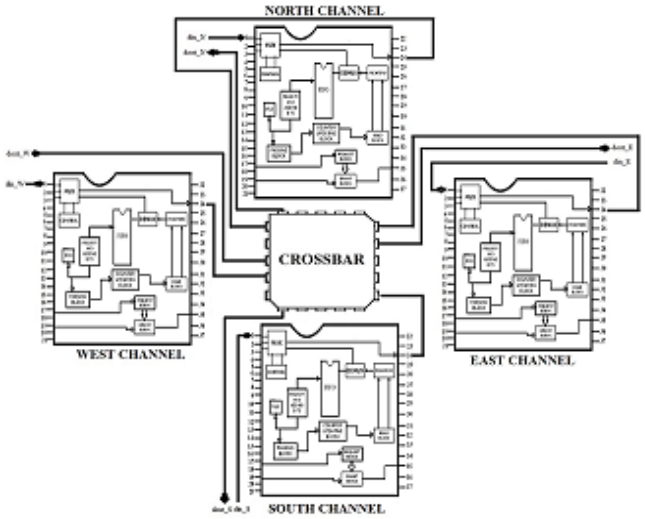

Fig. 1. Proposed Heterogeneous Router Architecture

A. Design of F.I.F.O

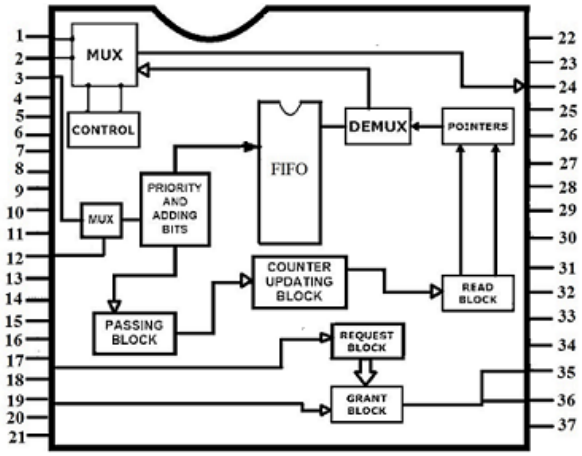

Fig. 2. Input FIFO in South Channel.

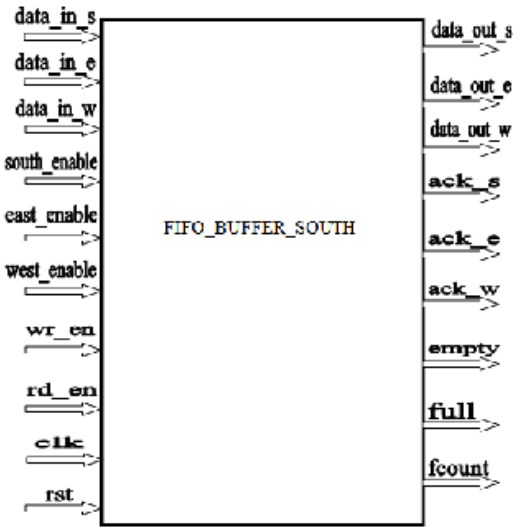

Fig. 3. Block Diagram of F.I.F.O

In Fig.2. shows exlicit view of south channel. Other channels also contain same architecture, FIFO decides the communication can start or not. If the FIFO is empty the data can be written in it and communication can start. If FIFO is full, data can be forwarded to its destination router. The read and write operation of FIFO is controlled by control logic. The word length considered in the above FIFO is 8-bits that can be changed as per the design.

Read counter (rd_en) and write counter (wr_en) are the variables which stores number of read and write operation on the FIFO buffers. These variables are used to know whether the FIFO is empty or full. data_in_s corresponds to data that's an input to south fifo while data_in_e and data_in_w are the data coming from right buffer & left buffer respectively that too in reference with south buffer.

data_out_s is the data output from south buffer that via channel flow goes to crossbar and is ousted with the logic applied. Data_out_e and data_out_w are respectively east and west buffers' data headed to their own buffer respectively.ack_s, ack_e and ack_w are acknowledgement signals.south_enable: for accepting data I/P of south fifo itself.east_enable: for accepting data I/P of east fifo.west_enable: for accepting data I/P of west fifo.rst stands for reset that reckons buffer into its initial state. clk stands for clock supplied to the whole design.

B. Channel / control logic:

SOUTH	SOUTH
SOUTH	WEST
WEST	SOUTH
WEST	EAST
EAST	EAST
EAST	WEST
~~SOUTH~~	SOUTH
~~SOUTH~~	WEST

Fig .4. Original and Proposed channel intake

The channel I Fig.4. of the proposed router supports heterogeneous data by storing again its own data i.e. heterogeneous data in comparision to layered data in original router.

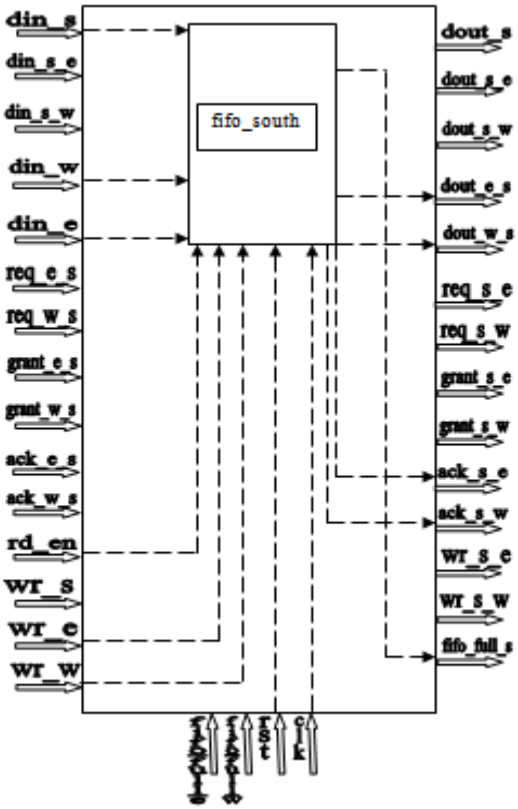

Fig.5. South Channel

Fig.5. shows South Channel Flow or Control Logic controls the arbitration of the ports and resolves contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports

are communicating with each other. Packets with the same priority and destined for the same output port are scheduled. Supposing in a given period of time, there was many input ports request the same output or resource, the Channel Flow or Control Logic is in charge of processing the priorities among many different request inputs. The Channel Flow or Control Logic will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of control logic.

When an input channel is connected to an output channel, the flits are sent one-by-one, and the pointers are updated as each flit is sent. Each channel knows how many buffer slots it has allocated, when the pointers present an address belonging to a neighbor buffer slot, the control logic allows the sending of the respective flits to the output of its channel. As we do not change the routing policy, there is no possibility of entering a deadlock situation. Of course, one could be concerned about one channel asking buffers from another channel which is also asking for buffers. Since only the neighbors are asked about lending/borrowing, no cycle can be made, and hence at the circuit level there is also no possibility of deadlock.

C. Crossbar Switch

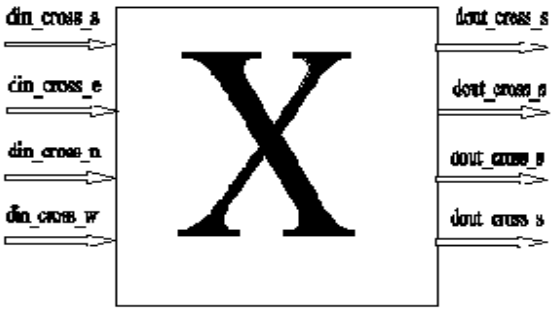

Fig. 6. Crossbar Switch

As shown in Fig.6. crossbar switch (also known as cross-point switch, crosspoint switch, or matrix switch) is a switch connecting multiple inputs to multiple outputs in a matrix manner. The design of the crossbar switch used in our design has 4 inputs and 4 outputs.

din_cross_s, din_cross_e, d din_cross_n, din_cross_w are the data coming from south, east, north & west fifos' respectively via channel flow or control logic.

Crossbar logic selects the data as per the programmed logic circuitry and ousts through dout_cross_s, dout_cross_e, dout_cross_n, dout_cross_w ports.

D. Complete reconfigurable router:

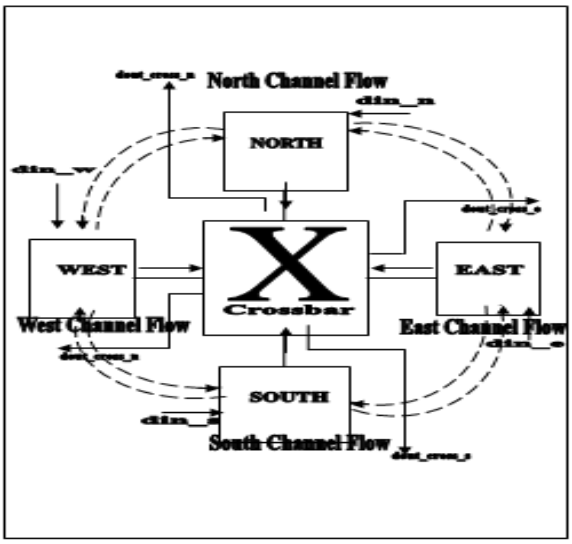

Fig.7. Reconfigurable N.O.C Router with channel flow.

Fig.7. shows complete Reconfigurable router with south , east , north , west channels flow.

V. Results

A. FIFO

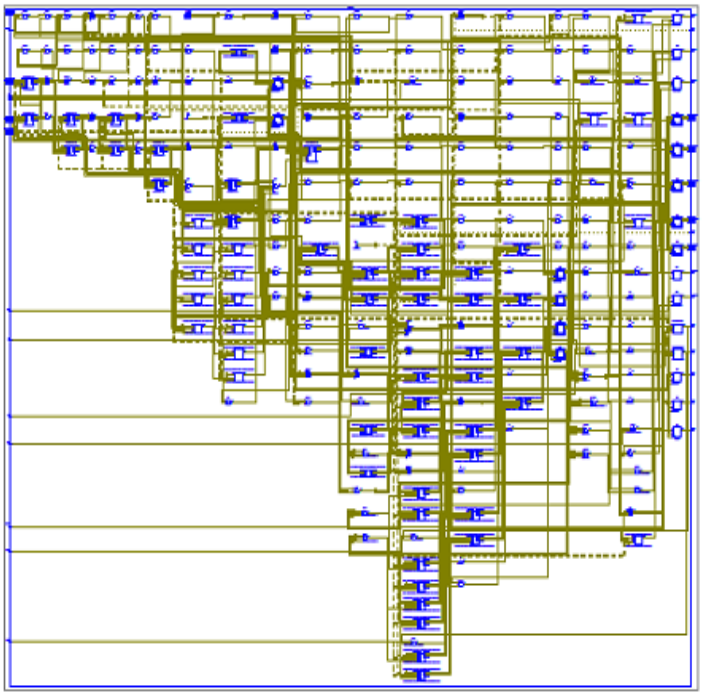

Fig.8. RTL view of F.I.F.O

B. Channel Flow/Control Logic

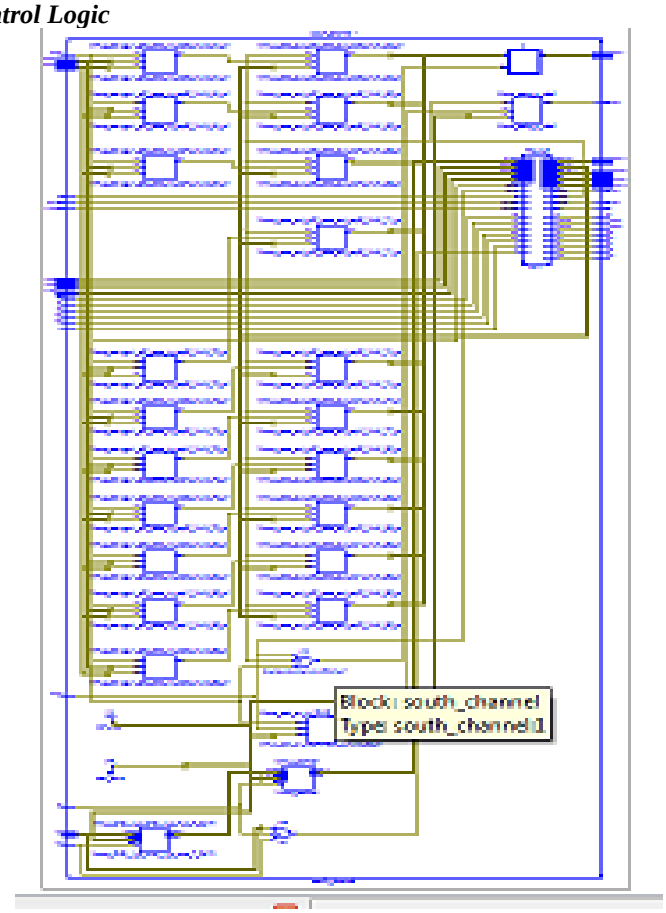

Fig.9. RTL view of South Channel

C. Crossbar

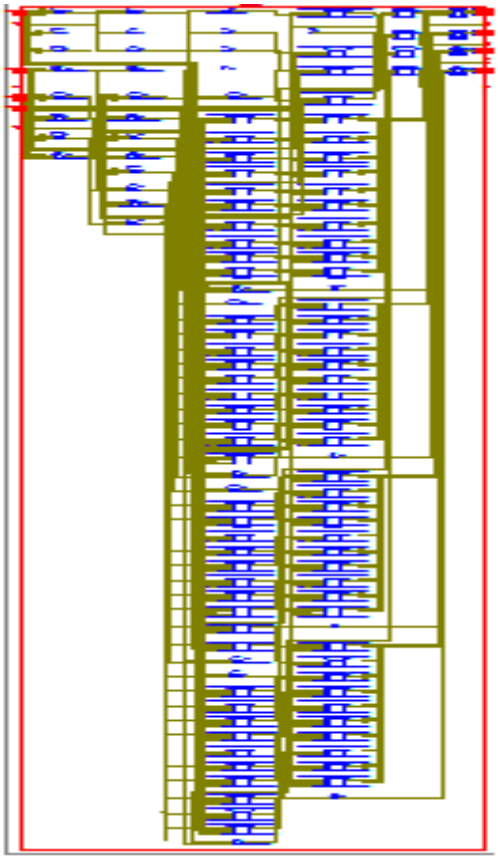

Fig.10. RTL view of Crossbar

D. Simulation of proposed router.

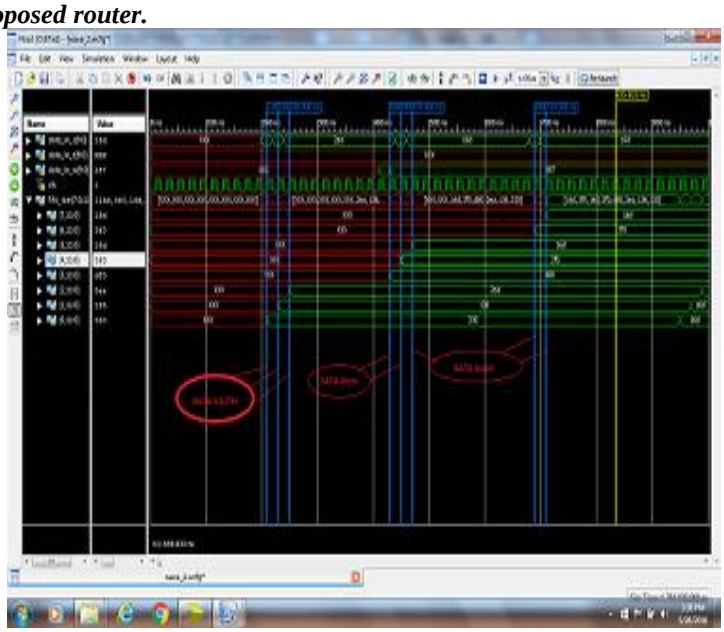

Fig. 11. Complete south channel waveform showing Heterogeneous data.

Output waveform of the complete south channel is shown in Fig. 11. All the four channels are connected to crossbar switch because final output is taken from the crossbar.It shows heterogeneous storage of data by storing south data twice.

Fig. 11, shows how FIFO buffer of south, west & east occupies by data value. Waveform of store value in South, East, West channels are shown. The stored value of south, east, and west FIFO Stack is shown . The final output of south channel is taken and connected to the crossbar switch.

E. Design utilization summary.

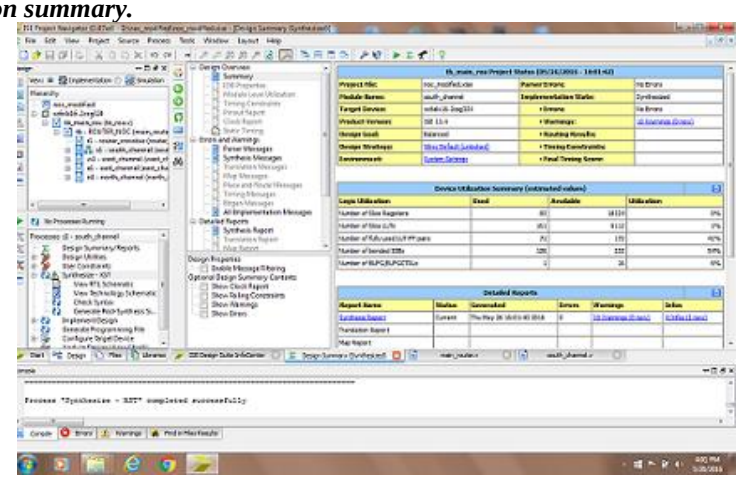

Fig. 12. Design Utilazation summary of South Channel .

Fig.12. shows the device utilization summary of south channel in terms of number slice registers , LUT'S , bonded IOB's .

F. Power analysis by xilinx power analyzer tool (xpa).

Xilinx Power Analyzer (XPA) is a design tool used to analyze real design data. It is used to calculate power after design implemented in Xilinx ISE software. It uses the NCD file output from Place & Route (PAR) step.

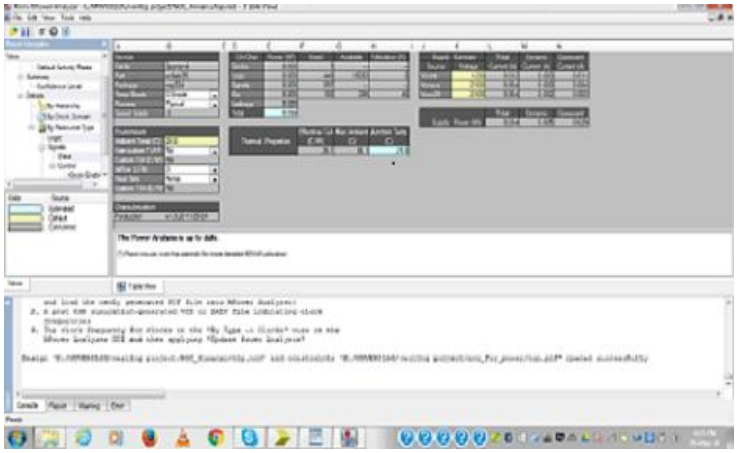

Fig.13 . Power summary of original reconfigurable router .

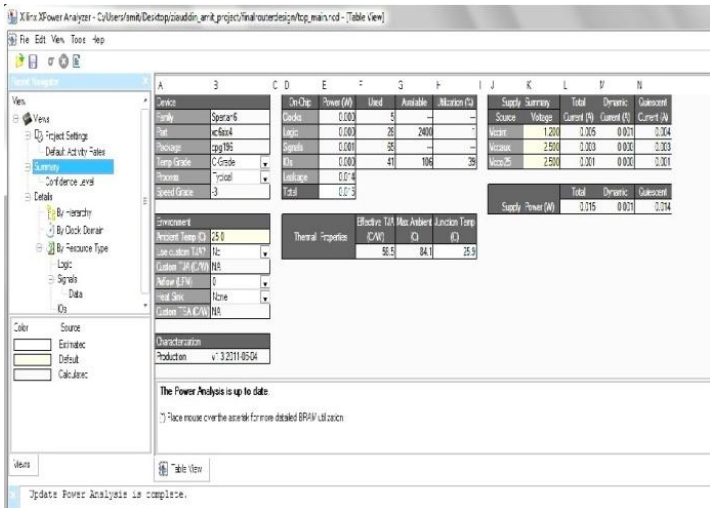

Fig. 14. Power summary of proposed heterogeneous router

G. Power Calculation

Calculation of total power dissipation of complete router architecture is done with the help of XPower Analyzer in Xilinx ISE 13.4. For this purpose FPGAs Kit (Spartan-6) is used. The total power is calculated at a frequency of 100 MHz. Obtained results are shown in Fig. 13. It is obvious from Fig. 13 that total power dissipated by the original router architecture is 20 mW. Total power for our proposed heterogeneous reconfigurable router is 15mW as shown in Fig.14 . Hence power is reduced by 5mW in our proposed architecture.

VI. Conclusion

In this project, the advantage of the use of an NoC with reconfigurable routers instead of homogeneous ones has been documented and simulated. Using reconfiguration, one can dynamically change the buffer depth to each channel, in accordance to the necessity of the application at same performance level. It was tested via simulation & verified that to reach the same performance obtained with the reconfigurable router, the original architecture, i.e. homogeneous router needs many more buffers.

The new router, while reaching the same performance than the original architecture, can obtain a reduction of power consumption though it can be tested via power measuring software tool that has been prevailed for concept of future work. Moreover, the reconfigurable router obtains the same performance of the homogeneous router with a comparatively less area .

Moreover, with the new architecture it is possible to reconfigure the router in accordance with the application, obtaining similar performances even when the application radically changes.

References

[1]. L. Benini and G. De Micheli, "Network on chips: A new SoC paradigm," *IEEE Computer*, vol. 35, no. 1, pp. 70–78, Jan. 2002.
[2]. M. Azimi, N. Cherukuri, D. N. Jayasimha, A. Kumar, P. Kundu, S.Park, I. Schoinas, and A. S. Vaidya, "Integration challenges and tradeoff for tera-scale architectures," *Intel Technol. J.*, vol. 11, no.3, Aug. 2007.
[3]. L. Manferdelli, N. K. Govindaraju, and C. Crall, "Challenges and opportunities in many-core computing," *Proc.IEEE*, vol. 96, no. 5, pp. 808–815, May 2008.
[4]. C. Xuning and L. Peh, "Leakage power modeling and optimization in interconnection networks," in *Proc. Int. Symp. Low Power Electron. Des. (ISLPED)*, 2003, pp. 90–95.
[5]. T. Benini and G. De Micheli, "Analysis of power consumption on switch fabrics in network routers," in *Proc. 39th Des. Autom. Conf. (DAC)*, 2002, pp. 524–529.
[6]. C. Wu and H. Chi, "Design of a high-performance switch for circuit-switched on-chip networks," in *Proc. Asian Solid-State Circuits Conf.*, 2005, pp. 481–484.
[7]. S. E. Lee and N. Bagherzadeh, "Increasing the throughput of an adaptive router in network-on-chip (NoC)," in *Proc. Int. Conf. Hardw./Softw. Codes. Syst. Synth.*, 2006, pp. 82–87.
[8]. B. Ahmad, A. Ahmadinia, and T. Arslan, "Dynamically reconfigurable NOC with bus based interface for ease of integration and reduced designed time," in *Proc. NASA/ESA Conf. Adapt. Hardw. Syst. (AHS)*, 2008, pp. 309–314.